Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.   (previously presented) A method of detecting overflow in a clamping circuit, comprising:

inputting a first operand having a first fixed-point format into the clamping circuit;

inputting a second operand having a second fixed-point format into the clamping circuit;

determining an overflow output based upon the first and second fixed-point format and predicting whether an arithmetic operation of the first operand with the second operand will yield a result that exceeds the overflow output;

performing at least partially the arithmetic operation of the first and second operands;

inputting the result and overflow output into a multiplexor for selection therebetween; and

discontinuing the performing if the result exceeds the overflow output;

wherein the determining and predicting occurs independent from and substantially in parallel with the performing.

2.   (previously presented) A method of detecting overflow in a clamping circuit, comprising:

inputting a first operand having a first fixed-point format into the clamping circuit;

inputting a second operand having a second fixed-point format into the clamping circuit;

determining a product overflow output based upon the first and second fixed-point format and predicting whether multiplication of the first operand with the second operand yields a result that exceeds the product overflow output; and

performing at least partially the multiplication of the first and second operands;

inputting the result and product overflow output into a multiplexor for selection therebetween; and

discontinuing the performing if the result exceeds the product overflow output;wherein the determining and predicting occurs independent from and substantially in parallel with the performing.

3.   (currently amended) A method of clamping fixed-point multipliers, comprising:

    providing a first operand in a first fixed-point format;

    providing a second operand in a second fixed-point format;

    at least partially multiplying the first operand with the second operand to produce an operation result;

    determining whether the operation result will exceed a representable value;

    determining a clamping value based on the first fixed-point format of the first operand and the second fixed-point format of the second operand;

    substituting the operation result with the clamping value when it is determined that the operation result will exceed the representable value;

    ~~inputting the operation result into a multiplexor;~~ and

    discontinuing the multiplying if the operation result exceeds the representable value;

    wherein the multiplying and determining whether the operation result will exceed the representable value occur independently and substantially in parallel.

4.   (previously presented) A method of clamping fixed-point multipliers, comprising:

    providing a first and second input operand;

    determining a desired number of output bits;

    where any of the first and second input operands are positive, counting a number of leading logical zeros in the positive operands;

    where any of the first and second input operands are negative, counting a number of leading logical ones in the negative operands;

    summing the number of leading logical zeros of the positive operands with the number of leading logical ones in the negative operands;

    determining a clamping decision based on the summing to yield a simple clamp predictor representative of the clamping decision;

    computing a product of the first operand and the second operand such that the product has the desired number of output bits plus one additional bit; and

    logically ORing the simple clamp predictor with a most significant bit of the product.

5.   (previously presented) The method of Claim 4, wherein the computing and determining the clamping decision to yield the simple clamp predictor occur independently and substantially in parallel.

6.   (currently amended) A method of processing multiplier data paths, comprising:
        <u>selecting a rule for a multiplication operation;</u>
        performing at least a partial multiplication of a plurality of operands, each having a fixed-point format;
        determining whether the at least partial multiplication of the operands produces a product that will exceed a pre-determined limit based upon the fixed-point format of each of the operands;
        inputting the product into a multiplexor; and
        discontinuing the performing if the product exceeds the pre-determined limit;
        wherein the performance and the determining occur independently and substantially in parallel.

7.   (previously presented) A method of clamp detection, comprising:
        inputting a first and a second operand to both a multiplier and an overflow detection circuit;
        multiplying the first and second operands to generate a result not to exceed a pre-determined number of bits;
        determining an initial clamping predictor bit based upon the first operand and the second operand;
        logically ORing the initial clamping predictor bit and a most significant bit of the result to produce a final clamping predictor bit;
        inputting the result into a multiplexor; and
        discontinuing the multiplying if the result exceeds the pre-determined number of bits;
        wherein the multiplying and determining occur independently and substantially in parallel.

8.   (previously presented) The method of Claim 7, wherein the first and second operands are in a fixed-point format.

9.   (previously presented) A method of clamp detection, comprising:

inputting a first and a second operand to both a multiplier and an overflow detection circuit;

multiplying the first and second operands to generate a result not to exceed a predetermined number of bits;

determining an initial clamping predictor bit based upon the first operand and the second operand; and

logically ORing the initial clamping predictor bit and a most significant bit of the result to produce a final clamping predictor bit,

wherein the multiplying and determining occur independently and substantially in parallel,

wherein the most significant bit of the result is logically inverted prior to the logically ORing.

10.   (previously presented) A method of clamp detection, comprising:

inputting a first and a second operand to both a multiplier and an overflow detection circuit;

multiplying the first and second operands to generate a result not to exceed a predetermined number of bits;

determining an initial clamping predictor bit based upon the first operand and the second operand; and

logically ORing the initial clamping predictor bit and a most significant bit of the result to produce a final clamping predictor bit;

wherein the multiplying and determining occur independently and substantially in parallel;

wherein the first and second operands are in a fixed-point format; and

wherein determining the initial clamping predictor bit includes determining a number of logical zeros in each of the operands and summing the number of logical zeros to determine whether the sum exceeds a pre-determined number to determine the initial clamping predictor bit.

11.   (previously presented) A method of clamp detection, comprising:

inputting a first and a second operand to both a multiplier and an overflow detection circuit;

multiplying the first and second operands to generate a result not to exceed a pre-determined number of bits;

determining an initial clamping predictor bit based upon the first operand and the second operand; and

logically ORing the initial clamping predictor bit and a most significant bit of the result to produce a final clamping predictor bit;

wherein the multiplying and determining occur independently and substantially in parallel;

wherein the first and second operands are in a fixed-point format; and

wherein determining the initial clamping predictor bit includes determining a number of logical ones in each of the operands and summing the number of logical ones to determine whether the sum exceeds a pre-determined number.

12.   (previously presented) A method of clamp detection, comprising:

inputting a first and a second operand to both a multiplier and an overflow detection circuit;

multiplying the first and second operands to generate a result not to exceed a pre-determined number of bits;

determining an initial clamping predictor bit based upon the first operand and the second operand; and

logically ORing the initial clamping predictor bit and a most significant bit of the result to produce a final clamping predictor bit;

wherein the multiplying and determining occur independently and substantially in parallel;

wherein the first and second operands are in a fixed-point format; and

wherein determining the initial clamping predictor bit further comprises, when one of the operands is negative and one of the operands is positive, determining a number of logical ones for the negative operand and a number of logical zeros for the positive operand and summing the number of logical ones and the number of logical zeros to determine whether the sum exceeds or is equal to a pre-determined value for clamping to occur.

13.   (currently amended) A multiplication overflow detection circuit, comprising:

multiplication circuitry for at least partially multiplying a first and a second operand; and

overflow detection circuitry receiving the first and second operands that detects whether a result of the multiplication of the first and second operands exceed a maximum representable positive or negative value;

wherein the multiplication circuitry and the overflow detection circuitry operate independently and substantially in parallel;

the result is input into a multiplexor; and

the multiplying is discontinued if the result exceeds the maximum representable positive or negative value, wherein determining the initial clamping predictor bit includes determining at least one of a number of logical ones or a number of logical zeros in each of the operands and summing the number of logical ones or a number of logical zeros to determine whether the sum exceeds a pre-determined number.

14.   (previously presented) The circuit of Claim 13, wherein the overflow detection circuitry utilizes a fixed-point format of the first and second operands to determine whether the result of the multiplication exceeds the maximum representable positive or negative value.

15.   (previously presented) An overflow detection circuit, comprising:

a first register for storing a first operand;

a second register for storing a second operand;

overflow detection circuitry for detecting an overflow of a multiplication of the first operand and the second operand and producing a clamp bit;

a multiplier for at least partially multiplying the first and second operands and generating a result not to exceed a pre-determined number of bits;

a clamp bit register for storing the clamp bit from the overflow detection circuitry; and

a result register connected to the multiplier for storing the result of the multiplication of the first and second operands;

wherein the overflow detection circuitry and the multiplier operate independently and substantially in parallel;

the result is input into a multiplexor; and

the multiplying is discontinued if the result exceeds the pre-determined number of bits.

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16.   (previously presented) An overflow detection circuit, comprising:

a first register for storing a first operand;

a second register for storing a second operand;

overflow detection circuitry for detecting an overflow of a multiplication of the first operand and the second operand and producing a clamp bit;

a multiplier for at least partially multiplying the first and second operands and generating a result not to exceed a pre-determined number of bits;

a clamp bit register for storing the clamp bit from the overflow detection circuitry; and

a result register connected to the multiplier for storing the result of the multiplication of the first and second operands;

wherein the overflow detection circuitry and the multiplier operate independently and substantially in parallel, and

the multiplying is discontinued if the result exceeds the pre-determined number of bits,

the overflow detection circuit further comprising:

a multiplexer comprising:

a clamp value input for receiving a clamp value to be output when clamping occurs;

a clamp bit register input connected to the clamp bit register for receiving the clamp bit;

a result register input connected to the result register for receiving the result of the multiplication of the first and second operands; and

an output;

wherein the multiplexer selects one of the clamp value register input and the result register input based upon a logical level of the clamp bit register in order to make the selected input the output of the multiplexer.

17.   (currently amended) An overflow detection circuit, comprising:

a first register for storing a first operand;

a second register for storing a second operand;

overflow detection circuitry for detecting an overflow of a multiplication of the first operand and the second operand and producing a clamp bit;

~~a multiplier for at least partially multiplying the first and second operands and~~ generating a result not to exceed a pre-determined number of bits;

a clamp bit register for storing the clamp bit from the overflow detection circuitry; and

a result register connected to the multiplier for storing the result of the multiplication of the first and second operands;

wherein the overflow detection circuitry and the multiplier operate independently and substantially in parallel, the clamp bit input is logically ORed with a most significant bit of the result stored in the result register,

wherein the result is input into a multiplexor, ~~and~~

wherein the multiplying is discontinued if the result exceeds the pre-determined number of bits; and

a logic device processes the multiplexor output for pipelining.

18.   (currently amended) An overflow detection circuit, comprising:

a first register for storing a first operand;

a second register for storing a second operand;

overflow detection circuitry for detecting an overflow of a multiplication of the first operand and the second operand and producing a clamp bit;

a multiplier for at least partially multiplying the first and second operands and generating a result not to exceed a pre-determined number of bits;

a clamp bit register for storing the clamp bit from the overflow detection circuitry;

a result register connected to the multiplier for storing the result of the multiplication of the first and second operands,

wherein the overflow detection circuitry and the multiplier operate independently and substantially in parallel;

wherein the result is input into the multiplexor, wherein the pre-determined number of bits is a clamp value determined by a maximum representable positive or negative value; and

the multiplying is discontinued if the result exceeds the pre-determined number of bits. wherein at least one of the registers is a flip-flop.

19.   (previously presented) The overflow detection circuit of Claim 15, wherein the first and second registers store the first and second operands in a fixed-point format.

20.   (previously presented) The method of Claim 7, further comprising determining whether clamping occurs based upon a logical value of the final clamping predictor bit and selecting one of a pre-selected clamp value and the result of the multiplying.

21.   (new) The circuit according to Claim 18, wherein a clamp value is hardwired into the multiplexor.